## CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. (**Currently Amended**) Drive circuit for driving an output stage of a device for noise suppression, in particular in a motor vehicle, comprising:

- a first input for coupling in an unmodulated first clock signal of a first frequency,

- a second input for coupling in a PWM-modulated second clock signal of a second, lower frequency,

- a modulator circuit which from the first clock signal generates a PWM-modulated third clock signal of the first frequency which can be tapped at ~~the~~ **a** PWM output of the drive circuit, and

- a regulating circuit which regulates the pulse width of the third clock signal until ~~the~~ **a** sum of ~~the~~ **a** pulse duty factors of the second clock signal and of ~~the~~ **an** inverted third clock signal is 100%.

2. (**Currently Amended**) Drive circuit according to Claim 1, wherein the regulating circuit has an addresser**, wherein the regulating circuit** ~~which~~ generates a first regulating signal from the sum of the second clock signal and of the inverted third clock signal.

3. (Original) Drive circuit according to Claim 2, wherein the addresser has a first voltage divider whose resistors have the same conductance.

4. (Original) Drive circuit according to Claim 2, wherein the regulating circuit has a first comparator which generates the first regulating signal for driving the modulator circuit as a function of a difference between a reference potential and a summation signal generated by the addresser.

5. (**Currently Amended**) Drive circuit according to Claim 4, **wherein the addresser has a first voltage divider whose resistors have the same conductance and** wherein ~~**for generating**~~ the reference potential **includes** a second voltage divider ~~**is provided which is located**~~ **coupled** between ~~**terminals of**~~ a **voltage** supply ~~**voltage source**~~**and ground**.

6. (Original) Drive circuit according to Claim 1, wherein the regulating circuit is designed as a PID regulator and/or as an I regulator.

7. (**Currently Amended**) Drive circuit according to Claim ~~**1**~~**4**, wherein the modulator circuit has a NAND gate, a downstream ramp generator, second comparator, and flip-flop.

8. (Original) Drive circuit according to Claim 7, wherein the ramp generator has a switchable current source and an integration capacitor for generating a ramp voltage.

9. (**Currently Amended**) Drive circuit according to Claim 7, wherein the second comparator is connected on the input ~~**side**~~ **sides** to the output of the ramp generator and to the output of the regulating circuit, ~~**with**~~ **wherein** the second comparator comparing the ramp voltage with ~~**the**~~ **a** first regulating signal and, ~~**as a function of this,**~~**for** generating a trigger signal for triggering the flip-flop.

10. (**Currently Amended**) Drive circuit according to Claim 7, wherein the flip-flop is connected on the input ~~**side**~~ **sides** to the first input and to the output of the second comparator, ~~**with**~~ **wherein** the flip-flop ~~**making**~~ **produces at the output** the third clock signal and a clock signal inverted with respect to ~~**this**~~ **the third clock signal** ~~**available at the output**~~ as a function of the trigger signal and of the first clock signal.

11. (**Currently Amended**) Drive circuit according to Claim 1, wherein the drive circuit is a ~~**component part of**~~**peripheral device within** a program-controlled unit, in particular ~~**of**~~ **within** a microcontroller or microprocessor.

12. (**Currently Amended**) Devices for electronic noise suppression, in particular for a motor vehicle comprising:

- a microphone for registering noises,
- a loudspeaker for feeding out acoustic signals for noise suppression,
- a circuit arrangement for driving the loudspeaker according to the registered noises which has a drive circuit for provisioning a PWM-modulated clock signal, comprising:

- a first input for coupling in an unmodulated first clock signal of a first frequency,

- a second input for coupling in a PWM-modulated second clock signal of a second, lower frequency,

- a modulator circuit which from the first clock signal generates a PWM-modulated third clock signal of the first frequency which can be tapped at ~~**the**~~ **a** PWM output of the drive circuit, and

- a regulating circuit which regulates the pulse width of the third clock signal until ~~**the**~~ **a** sum of ~~**the**~~ **a** pulse duty factors of the second clock signal and of ~~**the**~~ **an** inverted third clock signal is 100%,

and

- an output stage which is connected immediately downstream of the drive circuit and which drives the loudspeaker.

13. (Original) Device according to Claim 12, wherein the output stage is designed as a class D amplifier.

14. (Original) Device according to Claim 12, wherein the output stage has a driver circuit and a bridge circuit, in particular a full bridge, which is connected downstream of the driver circuit.

15. (**Currently Amended**) Device according to Claim 12, wherein a program-controlled unit, in particular a microcontroller or microprocessor, is provided which is connected immediately upstream of the driver circuit or which ~~has~~ **includes** the driver circuit.

16. (Original) Device according to Claim 12, wherein the output stage is driven directly by a microcontroller.

17. (**Currently Amended**) Method for driving an output stage of a device for noise suppression, in particular in a motor vehicle, comprising the steps of:

- generating from an unmodulated first clock signal of a first frequency and from a PWM-modulated second clock signal of a second frequency, which is lower than the first frequency, a PWM-modulated third clock signal of the first frequency whose pulse duty factor continues being increased on a regulated basis until ~~the~~ **a** sum of ~~the~~ pulse duty factors of the second clock signal and of ~~the~~ **an inverted** third clock signal is 100%,
- using the frequency of the first clock signal as a control variable, and
- using the third clock signal ~~made available on the output side~~ as a regulating variable for regulation.

18. (Original) Method according to Claim 17, wherein the first and/or second clock signal are/is made available by a program-controlled unit.

19. (Original) Method according to Claim 17, wherein a flip-flop is used for generating the pulse width of the PWM-modulated third clock signal.

20. (**Currently Amended**) **A method according to Claim 17, comprising the step of** ~~Use~~ **using**~~of~~ a microprocessor or microcontroller for directly driving an output stage, in particular a class D output stage, with a PWM-modulated clock signal in **the**~~a~~ device for electronic noise suppression.